Claim Amendments

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) A content addressable memory, comprising:

at least one tag input;

at least one random access memory;

circuitry to:

perform multiple read operations of the at least one random access memory for multiple, different ones of the read operations specifying an address based on different subsets of tag bits; and

digital logic circuitry coupled to the at least one random access memory, the circuitry including digital logic gates to:

determine whether a lookup tag matches one or more entries represented by data stored in the random access memory based on each of the different subsets of the tag bits;

determine whether a portion of the lookup tag matches a portion of one or more entries represented by the data stored in the random access memory based on **[[a]]** less than all ~~subset~~ of the different subsets of tag bits; and

simultaneously outputting (1) at least one match signal based on whether the lookup tag matches one or more entries represented by the data stored in the random access memory based on each of the different subsets of

the tag bits and (2) at least one match signal based on whether the portion of the lookup tag matches a portion of one or more entries represented by the data stored in the random access memory based on less than all of the different subsets of the tag bits.

2. (currently amended) The content addressable memory of claim 1,

wherein the digital logic ~~network~~ circuitry further comprises digital logic gates to determine whether a lookup tag matches all of the different subsets of tag bits.

3. (original) The content addressable memory of claim 1,

wherein the circuitry comprises multiple networks of digital logic gates, individual ones of the networks operating on the same bit-positions of data output by the at least one random access memory.

4. (original) The content addressable memory of claim 3,

wherein the individual networks comprise a tree of AND gates.

5. (currently amended) The content addressable memory of claim 4,

wherein the circuitry comprises an OR-gate ~~feed~~ fed by the networks.

6. (original) The content addressable memory of claim 1,

wherein the circuitry comprises digital logic including a NOT operation.

7. (original) The content addressable memory of claim 1, wherein the at least one random access memory comprises multiple random access memories.

8. (currently amended) The content addressable memory of claim 7,

wherein the number of tag subsets used in the multiple read operations is equal to the number of random access memories **[[;]]** .

9. (original) The content addressable memory of claim 8,

wherein each of the tags subsets forms an address applied to each of the respective random access memories.

10. (original) The content addressable memory of claim 9,

wherein the multiple read operations comprise more than one read operation applied to the same random access memory.

11. (original) The content addressable memory of claim 1, wherein the circuitry is constructed to perform at least two of the read operations in parallel.

12. (original) The content addressable memory of claim 1,

wherein the circuitry further comprises circuitry to write bits to the at least one random access memory in response to a tag value to be written to the content addressable memory.

13. (currently amended) The content addressable memory of claim 12,

wherein the ~~ternary~~ tag value to be written comprises a tag value including at least one "don't care" bit; and

wherein the circuitry to write bits comprises circuitry to set bits for different subsets of tag values occupying the same bit positions.

14. (currently amended) A method, comprising:

dividing a received content addressable memory lookup tag value into multiple subtags ~~values~~;

performing multiple read operations of at least one random access memory using addresses based on the multiple, respective, subtags ~~subtag values~~;

determining whether the lookup tag matches one or more entries represented by data stored in the at least one random access memory based on each of the multiple subtags;

determining whether a portion of the lookup tag matches a portion of one or more entries represented by the data stored in the at least one random access memory based on less than all of the multiple subtags; and

simultaneously outputting (1) at least one match signal based on whether the lookup tag matches one or more entries represented by the data stored in the random access memory based on each of the multiple subtags and (2) at least one match signal based on whether the portion of the lookup tag matches a portion of one or more entries represented by the data stored in the random access memory based on less than all of the multiple subtags

~~based on the read operations, determining which, if any, entries feature a subset of the multiple subtags; and~~

~~outputting at least one indication in response to the determining~~.

15. (original) The method of claim 14, wherein performing multiple read operations comprises using each of the multiple subtags as at least a portion of an address specified in the read operations.

16. (original) The method of claim 14, wherein the at least one random access memory comprises multiple random access memories.

17. (currently amended) The method of claim ~~19~~ 16, wherein the multiple random access memories store a bit vector of entry values at the subtag addresses.

18. (original) The method of claim 14, further comprising:

receiving a tag to write; and

setting bits in the at least one random access memory based on the received tag.

19. (original) The method of claim 18,

wherein receiving a tag comprises receiving a tag including at least one "don't care" bit; and

wherein the setting bits comprises writing entry data associated with multiple values of the same subtag within a one of the at least one random access memories.

20. (currently amended) A network forwarding device, comprising:

a switch fabric; and

multiple line cards interconnected by the switch fabric, individual ones of the line cards comprising:

at least one network port; and

circuitry to process packets received via the at least one port, the digital logic circuitry including a content addressable memory, the content addressable memory comprising:

at least one tag input;

at least one output;

at least one random access memory;

content addressable memory circuitry to:

perform multiple read operations of the at least one random access memory for multiple, different ones of the read operations specifying an address based on different subsets of tag bits; and

digital logic circuitry coupled to the at least one random access memory, the circuitry including digital logic gates to :

determine whether a lookup tag matches one or more entries represented by data stored in the random access memory based on each of the different subsets of the tag bits;

determine whether a portion of the lookup tag matches a portion of one or more entries represented by the data stored in the random access memory based on [[**a**]] less than all ~~subset~~ of the different subsets of tag bits; and

simultaneously outputting (1) at least one match signal based on whether the lookup tag matches one or more entries represented by the data stored in the random access memory based on each of the different subsets of the tag bits and (2) at least one match signal based on whether the portion of the lookup tag matches a portion of one or more entries represented by the data stored in the random access memory based on less than all of the different subsets of the tag bits.

21. (original) The network forwarding device of claim 20, wherein at least one of the line cards comprises a network processor having multiple multi-threaded engines integrated on a single die.